4E Power Electronic Conversion Technology Annex PECTA.

Task B: Energy and environmental related Life Cycle Assessment (LCA).

Paper publication: *A "life cycle thinking" approach to assess differences in the energy use of SiC vs. Si power semiconductors.*

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This paper presents the outcomes of the work from Area 1 of PECTA Task B, Energy and environmental related Life Cycle Assessment, conducted between January and September 2021. See more information under: https://www.iea-4e.org/pecta/tasks/.

The scope is the production of Wide Band Gap (WBG) semiconductors and the assessment of environmental aspects is focusing on the energy use for the different manufacturing processing steps. This investigation is especially relevant for Silicon carbide (SiC) semiconductors, as there are some key differences in production processes compared to (conventional) Silicon semiconductors. Through interviews with academic and industry expert and extensive literature research, this paper presents the main differences of the SiC semiconductors production chain.

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A “life cycle thinking” approach to assess differences in the energy use of SiC vs. Si power semiconductors.

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ABSTRACT:

Wide Band Gap (WBG) semiconductors have the potential to provide significant improvements in energy efficiency over conventional Silicon (Si) semiconductors. While the potential for energy efficiency gains is widely researched, the relation to the energy use during manufacturing processes remains insufficiently studied. This question is especially relevant for Silicon carbide (SiC) semiconductors, as there are some key differences in their production processes compared to Si. Through expert interviews and literature research, this paper aims to identify the main differences of the SiC semiconductors production chain. These differences are set off against a typical end-use scenario, to better understand the proportionality of energy inputs vs. efficiency gains. Furthermore, the most important variables in this assessment are highlighted.

1. INTRODUCTION

The broader application of WBG semiconductors for power electronics carries the promise of large energy savings in a range of different applications. Some of the sectors with the highest expected energy efficiency gains enabled by WBG semiconductors are photovoltaic systems (inverters), consumer electronics (power supplies), data centers (uninterrupted power supplies), and the electric automotive sector (drive-trains and charging infrastructure (Makoschitz et al. 2020). While these energy efficiency improvements from using WBG components compared to Si-components are widely researched and often promoted by manufacturers, the environmental impacts along the entire life cycle (beyond the use phase) are far less understood. Moreover, to the best knowledge of the authors, there is currently no Life Cycle Assessment (LCA) data available specifically focusing on WBG semiconductors, related research is generally scarce, and (publicly) available LCA information of sufficient level of detail and quality is limited or outdated. Most of the current LCA research available in the field of semiconductors focuses on Si-based semiconductors, especially logic and other IC chips (Wernet et al. 2016)). These references mostly contain aggregated data, which does not allow for separate analysis of individual processes and of their materials and energy inputs and outputs.

From a life cycle thinking perspective two aspects seem highly relevant. First, ICs like semiconductor memories, processors or logic chips are highly **energy intensive** to manufacture due to their complex design. Often manufacturing requires hundreds of processing steps. Secondly, the industry is changing and innovating rapidly, and therefore it is also especially competitive and secretive. ICs are subject of a continuous process of miniaturization- also called “die shrink”. Boyd states that this is leading to a *continuous shift of* ***relevance*** *from the manufacturing stage to the use phase* (Boyd 2012).

These aspects do not fully apply to **power** semiconductors, such as metal oxide semiconductor field-effect transistors (MOSFETs) and diodes, as they are relatively less complex to produce, and are also less affected by the same continuous process of miniaturization. Taking on from these preliminary considerations, the next section discussed the specific assessment methodology and scope developed in this study. The key words to keep in mind are “relevance” and “differences”.

2. METHODOLOGY AND SCOPE

Available studies report that the electricity use in manufacturing is, after the use phase, the most important source of environmental impacts for Silicon based semiconductors (Williams et al. 2002; Yao et al. 2004). The approach of this paper is therefore to gain a better understanding of the differences in the energy demand (i.e., primarily electricity) along the whole life cycle for selected WBG power semiconductors.

This analysis started off by focusing on the two currently most widespread WBG semiconductor materials - Gallium nitride (GaN or Si/GaN) and Silicon carbide (SiC). However, initial research revealed that the detailed assessment of energy use and energy savings along the life cycle is particularly relevant for SiC semiconductors.

The methodology of this study is structured along the life cycle stages and the scope was set on understanding which **processes and/or life cycle stages were (most) relevant**, in two ways: (1) stages that are most important *in terms of their energy inputs*, and (2) stages where *significant differences exist between Si and SiC technologies*. This was achieved through literature review and by conducting targeted interviews with academic and industry experts; who are mostly contributors to IEA 4E PECTA[1]. Interviewed experts helped identify, verify and quantify key selected variables related to processes and their differences (PECTA AAG/IAG 2021, interview). Figure 1 shows an overview of the life cycle stages for SiC and Si-based power semiconductors in the scope of this study. A photovoltaic (PV) inverter was the end use application chosen for this paper given the relevant energy savings potential reported for the SiC-based (PV) inverters (Makoschitz et al. 2020).

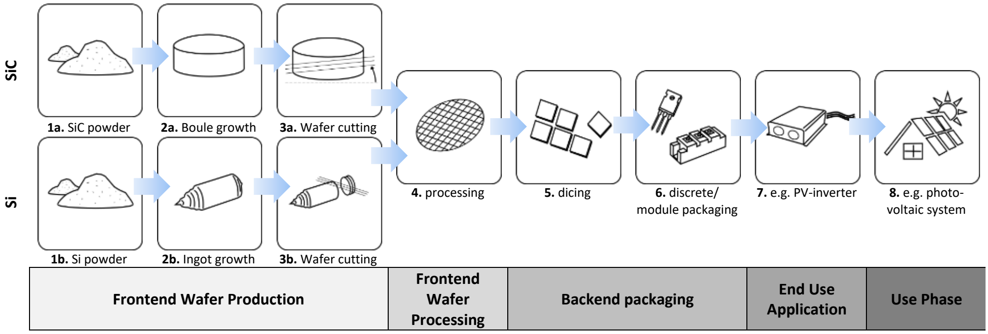

Figure 1: Life cycle stages of Si and SiC power semiconductors (Graphic: Schmidt, S. and S. Glaser (2021), own illustration).

RESULTS - DIFFERENCES ALONG THE LIFE CYCLE

The insights and results are discussed next for the processes and stages in Figure 1. It is important to mention that processes that are similar for both, Si and SiC, might have a substantial share of the overall energy demands. Still, the End of life stage of the electronic devices with SiC and Si is very similar at this point, and as such is not further investigated.

Front-End Wafer production: Si and most GaN semiconductors are manufactured using high purity industrial grade Silicon, by growing **Si ingots** through the Czrochalski process (Figure 1, 1b and 2b), with typical diameters of 8 to 12 inches (200mm and 300mm) (Prakash et al. 2011).

The substrate material for SiC semiconductors is also based on silica sand, with additional processing steps needed to obtain the SiC powder (Figure 1, step 1a). Usually, the Acheson process using physical vapor transport method (PVT) is applied. In this

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[1] PECTA is the **Power Electronic Conversion Technology Annex** of the IEA Energy Efficient End-Use Equipment Program (4E). Its goal is gathering and analysing information on new WBG power electronic devices to inform policy makers; see: https://www.iea-4e.org/pecta.

method, a graphite crucible is heated by induction coils to over 2300K in a furnace filled with a mixture of silica sand and carbon powder (Yang et al. 2018). The resulting SiC is ground into SiC powder and used as input material for **growing a "SiC boule"** (Figure 1, 2a). The Acheson process is estimated to require 7700 kWh electrical energy per ton of input material (Tanaka 2011); while the estimate for grinding is 1500 kWh/ton of SiC powder.

The input mass of SiC powder for growing a 6 inch (6") diameter SiC boule (usable height of 25mm) is about 30 kg; with a powder density of approx. 1,6g/cm^3. The estimated (embedded) energy of the input SiC powder is **280 kWh/boule** (Figure 1, 1a) (PECTA AAG/IAG 2021, interview).

In this study the reference is the production of 6" wafers. Taking the boule height of 25mm, with a growth rate of 0,2mm/h, and a power rating of 130kW (Ellefsen et al. 2019) for the growth process, the resulting energy demand is **16250 kWh/boule**. The growth of the boules (Figure 1, 2a) with its associated electricity demand, is one of the key performance indicators for the semiconductor´s energy profile.

As indicated before, reliable data regarding the energy demand for growing Si ingots was not available for this study (Most LCA data contain aggregated process data). It was therefore estimated that the energy demand is **20 to 40 times** higher per usable wafer area for growing SiC boules than for growing Si ingots (PECTA AAG/IAG 2021, interview).

In each case, the ingot and the boule are then cut into wafers (Figure 1, 3a and 3b), which are polished and prepared for further processing. Compared to Si ingots, SiC boules are much harder to cut into wafers (Armstrong et al. 2017). The process is also accompanied by significant "**kerf losses**", which are currently estimated to **range between 50% to 75%** (PECTA AAG/IAG 2021, interview). These are significantly higher losses than those from cutting Si ingots into wafers. Assuming low kerf losses of 50%, for a usable height of 25mm and 500µm wafer thickness after cutting would result in 25 wafers/per boule. Taking 100 kWh for the operation of the slicing equipment (1kW*100hr/boule), the resulting energy demand is **665kWh/6" unpolished SiC wafer**.

(Prakash et al. 2011) provide a specific estimate for the energy input for Si wafer production, with an electricity demand of 2127 kWh/kg of polished Si wafer. Converting this energy input estimation of the 6" Si wafer to calculate an equivalent 6" SiC wafer (from a 128g weight; and 8" wafer), and further assuming mass losses of 40% (due to polishing from a thickness of 500µm to 300µm), this results in an energy demand of **92kWh/6" equivalent unpolished Si wafer**; for a ratio of 1:7,22 (**92kWh [Si]**: **665kWh [SiC]**). As the assumptions behind the datasets are nt fully known, and the datasets are possibly outdated, the results for Si wafers shall be used with caution.

Front-end wafer processing: “Wafer processing” (Figure 1, step 4) strongly depends on the complexity of the final chip. ICs like semiconductor memories, processors or logic chips are at the end of the complexity spectrum, often requiring hundreds of wafer processing steps, with a range of different high purity chemicals applied to create layers or so called “**mask levels**”. Power semiconductors such as MOSFETs and diodes require far fewer mask levels compared to memories, processors or logic chips, e.g. SiC IGBTs (insulated-gate bipolar transistors) require about 11 to 12 mask levels (PECTA AAG/IAG 2021, interview).

Moreover, experts interviewed indicated that SiC wafer processing steps are very similar to Si wafer processing steps; therefore, these steps were not the focus of further investigation. However, one important difference is the processing yield. The yield is still lower for SiC wafers (due to crystal defects or process errors) than for the more established Si wafer front-end processing. The expert estimations for the overall front-end yield **is 75% for SiC, and 90% for Si** (PECTA AAG/IAG 2021, interview).

Back-end packaging: The back-end packaging processes follows the front-end processing and typically take place at a different manufacturing location. The dies on the processed wafer are cut into individual chips (Figure 1, step 5) and enclosed inside a protective package with external leads or connectors (Figure 1, step 6). There are about 20 families of different types of packages. The packaging type and the number of external leads are the most relevant variables for estimating the energy use of the back-end packaging process (Villard et al. 2015).

Due to the standardization of semiconductor packaging, the adoption of new packaging types is a slow process, which also depends on the device´s prevalence. As SiC devices are not yet widely common, they are usually packaged in the same types of packages as Si based devices. With SiC dies often being comparatively smaller than Si dies, using the same packaging type results in an overuse of packaging materials (PECTA AAG/IAG 2021, interview). Until new packaging standards are developed, it is plausible to consider the energy input for the back-end packaging process to be roughly the same for SiC as for Si semiconductors.

End-Use Application: The packaged chips or modules are incorporated into different end-use applications, e.g., in photovoltaic inverters (Figure 1, step 7). Key features of WBG devices play an important role. The higher switching frequencies and the lower energy conversion losses allow the design of compact and light weight end products with WBG semiconductors, consequently also using less materials. In the case of industrial transformers and power supplies with SiC, the **overall product size is reduced in the range of 25% to 50**% compared to equivalent Si applications (PECTA AAG/IAG 2021, interview). Certainly, the extent and relevance of this effect depends on the end-use application, and must be investigated at product level to understand how they translate into energy impacts. This will be further investigated in PECTA in the near future.

Use phase: This is the last life cycle stage covered in this study (Figure 1, step 8). Many studies have quantified the energy efficiency gains enabled by the introduction of WBG semiconductors, gains which vary widely depending on the end-use application. (Warren et al. 2015) estimate an average energy efficiency improvement of 14,7% due to the introduction of SiC semiconductors in the automotive industry (hybrid electric vehicles), resulting from improvements at the inverter level, but also from overall system improvements. For (PV) inverters, average energy efficiency gains of 2% are estimated (Makoschitz et al. 2020). As established Si based inverters already have a high efficiency in the order of 96,8%, further improvements seem rather limited.

In Austria PV systems have typically (approx.) 1000 hours of full load per year (use intensity). Assuming 20 years of service (product life time), the **efficiency gains,** namely the energy saved (not used) for a 1 MW (industry scale) PV system with a WBG inverter **would be approx. 20000 kWh/year, reaching up to 400000 kWh savings over its entire life cycle.** This example shows that the use of a WBG application could "pay back" many times the energy input needed for its manufacturing, through the higher efficiency and intense use over a long service life. In another scenario, the energy efficiency gains for power supplies in consumer electronics e.g., laptops, tablets and smartphones, range between 3% to 9% (Makoschitz et al. 2020).

KEY VARIABLES OF THE ENERGY PROFILE

The **five** most important aspects and variables for assessing the energy profiles and its differences between SiC and Si power semiconductors are discussed as follows:

(1) Boule growth: The growth of SiC boules requires significantly more energy per usable wafer area due the energy intensive processes, the smaller wafer diameters, and a significantly smaller usable height (thickness).

(2) Process yields: A number of losses influence the energy "burden" of the die at the end of the production line, notably the material losses for the growth of the boule (and ingot), the kerf losses from wafer cutting, and the processing losses due to faulty dies.

(3) Die size ratio: WBG power semiconductors are able to fulfil the same function with a smaller die. As growing the SiC boule is the most energy intensive step in the manufacturing, the die size ratio is key for assessing its energy profile.

(4) Effects on the product design: Using WBG semiconductors allowing higher switching frequency might have a strong impact on product design, enabling for example a reduction of material use, size and weight in selected end-use applications.

(5) Use phase characteristics: it is plausible to state that the Use phase of SiC power semiconductors will be the stage that plays the most important role, as shown with the

(PV) inverter example. Key variables in this case are the energy efficiency gains, the use intensity, and the product´s lifetime.

In summary, while the aspects 1 and 2 will negatively impact the energy profile of SiC devices (i.e., higher energy demand); the variables and aspects 3, 4 and 5 are those where SiC devices will show substantial improvements and savings.

4. DISCUSSION

As LCA data for WBG semiconductors was not readily available for this study, the aim was to describe the life cycle stages, the related processes and most relevant variables, especially for assessing their energy inputs. This study presented estimates of the energy inputs for four manufacturing steps (including sub-processes) of SiC and Si based devices, and discussed the differences in each case as well as their magnitude in relation to the potential for energy savings, taking as example a (SiC based) PV inverter as end-use application. The front-end processing and back-end packaging processes are very similar for both SiC and Si semiconductors. The front-end wafer production shows though more differences in terms of energy use, due to the nature of materials and the maturity of the processes involved (i.e., level of process losses). Further exploring the impacts on the design and on energy improvements resulting from incorporating SiC in certain end-use applications remains an area of research interest.

In terms of the life cycle thinking perspective presented in this study, future work aims at gaining a deeper understanding of the contribution to the life cycle stages that showed more differences between technologies as well as higher impact, to identify effective levers for improvement - a difficult task in light of the sparse LCA data available. Taking as references other relevant (LCA) impacts already identified for Si based semiconductors, i.e., global warming potential, abiotic resources depletion, water eutrophication, raw water use, human eco-toxicity, and photochemical (Summer) smog (Villard et al. 2015); the focus could also be expanded to assess these (LCA) impact categories for SiC semiconductors. Finally, research on the energy and environmental impacts of GaN based semiconductors will be pertinent, as these mature and penetrate the market.

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REFERENCES

Armstrong K, Das S, Marlino L, 2017. Wide Bandgap Semiconductor Opportunities in Power Electronics, US Dept. of Energy. https://info.ornl.gov/sites/publications/Files/Pub104869.pdf

Boyd S, 2012. Life-Cycle Assessment of Semiconductors (1. Aufl.). Springer New York, New York, NY, Online-Ressource.

Ellefsen OM, Arzig M, Steiner J, Wellmann P, Runde P, 2019. Optimization of the SiC Powder Source Material for Improved Process Conditions During PVT Growth of SiC Boules. Materials (Basel, Switzerland), 12 (19), 3272.

Makoschitz M, Krischan K, Bergmann P, Diaz A, Brueninger R, 2020. Wide Band Gap Technology: Efficiency Potential and Application Readiness Map. 4E PECTA, https://www.iea-4e.org/wp-content/uploads/publications/2020/05/PECTA_Report_Total-V10final-May-2020.pdf.

(PECTA AAG/IAG - Academic and Industrial Advisory Groups), 2021. Expert Interviews on WBG semiconductors and Si based semiconductors. Interview, 2021.

Prakash S, Schischke K, Stobbe L, 2011. Schaffung einer Datenbasis zur Ermittlung ökologischer Wirkungen der Produkte der Informations- und Kommunikationstechnik. Ressourcenschonung im Aktionsfeld IKT, unpublished.

Tanaka H, 2011. Silicon carbide powder and sintered materials. Journal of the Ceramic Society of Japan, 119 (1387), 218–233.

Villard A, Lelah A, Brissaud D, 2015. Drawing a chip environmental profile. Journal of Cleaner Production, 86, 98–109.

Warren JA, Riddle ME, Graziano DJ, Das S, Upadhyayula VKK, Masanet E, Cresko J, 2015. Energy Impacts of Wide Band Gap Semiconductors in U.S. Light-Duty Electric Vehicle Fleet. Env. Science & Technology, 49 (17), 10294–10302.

Wernet G, Bauer C, Steubing B, Reinhard J, Moreno-Ruiz E, Weidema B, 2016. The ecoinvent database version 3 (part I): overview and methodology. The Int. Journal of Life Cycle Assessment, 21 (9), 1218–1230.

Williams ED, Ayres RU, Heller M, 2002. The 1.7 kilogram microchip: energy and material use in the production of semiconductor devices. Env. Science & Technology, 36 (24), 5504–5510.

Yang C, Liu G, Chen C, Hou Y, Xu M, Zhang Y, 2018. Numerical Simulation of Temperature Fields in a Three-Dimensional SiC Crystal Growth Furnace with Axisymmetric and Spiral Coils. Applied Sciences, 8 (5), 705.

Yao MA, Wildson AR, Mcmanus TJ, Shadman F, 2004. 2004 IEEE Int. Symposium on Electronics & the Environment.10-13 May, 2004, Scottsdale, AZ, USA. IEEE, Piscataway, NJ, 328 p.

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